APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/458,370	12/09/1999	LOUIS A. LIPPINCOTT	10559/105001	8772

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FISH & RICHARDSON, PC
4350 LA JOLLA VILLAGE DRIVE
SUITE 500
SAN DIEGO, CA 92122

EXAMINER
HESSELTINE, RYAN J

ART UNIT	PAPER NUMBER
2623	

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____ .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-27_ is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-27_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on _09 December 1999_ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

     If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a) ☐ All b) ☐ Some * c) ☐ None of:

         1. ☐ Certified copies of the priority documents have been received.

         2. ☐ Certified copies of the priority documents have been received in Application No. _____ .

         3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

     a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1.   Figures 1-6 should be designated by a legend such as --Prior Art-- because only that

which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected

drawings are required in reply to the Office action to avoid abandonment of the application. The

objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.   Claims 1-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al.

(USPN 5,268,853), hereafter Tanaka.

4.   Regarding claims 1 and 8, Tanaka discloses a method/program for implementing a two-

dimensional inverse discrete cosine transform, comprising: executing two one-dimensional

inverse discrete cosine transforming functions, each of the functions being controlled to operate

on a matrix of coefficients in either of two different directions (column 5, line 12-17).

5.   Regarding claims 15 and 19, Tanaka discloses a method of implementing a two-

dimensional inverse discrete cosine transform (column 5, line 12-17), comprising: executing a

first one-dimensional inverse discrete cosine transforming function in a first direction on a first

matrix of coefficients to produce a matrix of intermediate and executing a second one-

dimensional inverse discrete cosine transforming function in a second, different direction on the

matrix of intermediate results concurrent with the first function executing in the second direction on a second matrix of coefficients (column 11, line 58 to column 12, line 10).

6. Regarding claims 23 and 25, Tanaka discloses an apparatus/computer implementing a two-dimensional inverse discrete cosine transform, comprising: two one-dimensional inverse discrete cosine transform blocks (figure 11, elements 4 and 6); a memory block (figure 11, elements 2a and 2b); a sequencer block, the sequencer block alternately being in one of two states, each state indicating the direction each one-dimensional inverse discrete cosine transform block operates in (figure 11, elements 20 and 22; column 6, line 50-55); and an address generator block (figure 5, element 8; column 6, line 56-65).

7. Regarding claim 27, Tanaka discloses a method of implementing a two-dimensional inverse discrete cosine transform, comprising: executing two one-dimensional inverse discrete cosine transforming functions to operate on a sequence of matrices, some matrices being operated on first in row order, then in column order and some matrices being operated on first in column order, then in row order (column 15, line 10-28).

8. Regarding claims 2, 9, 16, and 20, Tanaka discloses that one of the directions is row order (column 7, line 66-68).

9. Regarding claims 3, 10, 17, and 21, Tanaka discloses that one of the directions is column order (column 7, line 66-68).

10. Regarding claims 4 and 11, Tanaka discloses that a sequencer determines which direction each function operates in for a given matrix (figure 6, element 18; column 11, line 16-17).

11. Regarding claims 5 and 12, Tanaka discloses that an address generator generates an address for each coefficient in the matrix (column 5, line 55-59).

12.   Regarding claims 6 and 13, Tanaka discloses that the IDCT functions are concurrently executed in the same direction on two different matrices of coefficients (column 12, line 4-10).

13.   Regarding claims 7 and 14, Tanaka discloses that the functions are concurrently executed in the same direction (column 12, line 4-10), the functions switching periodically and concurrently to the other direction (column 15, line 10-28).

14.   Regarding claims 18 and 22, Tanaka discloses that the functions switch periodically and concurrently between the first and second directions (column 15, line 10-28).

15.   Regarding claims 24 and 26, Tanaka discloses that the address generator block is to generate addresses for the one-dimensional inverse discrete cosine transform blocks in the direction indicated by the state of the sequencer (column 11, line 16-40).

Conclusion

16.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- USPN 5,741,412 to Shyu discloses a recycling and parallel processing method and apparatus for performing discrete cosine transform and its inverse.

- USPN 5,481,487 to Jang et al. discloses transpose memory for DCT/IDCT circuit.

- USPN 5,541,658 to Ishiwata discloses image coding-decoding apparatus with efficient memory access.

- USPN 5,568,278 to Nakano et al. discloses image data coding and decoding method and apparatus with a plurality of DCT's, quantizers, and VLC's.

- USPN 5,737,256 to Nakagawa et al. discloses an inverse discrete cosine transform apparatus.
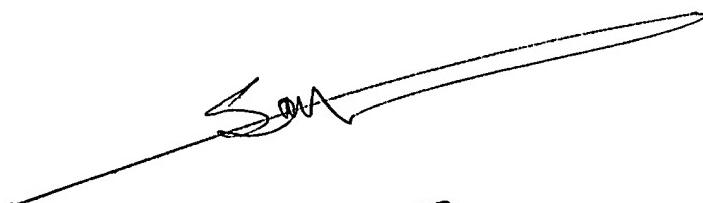
- USPN 6,011,498 to Wittig discloses a dual-speed variable length decoding architecture for MPEG-2 video data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan J Hesseltine whose telephone number is 703-306-4069. The examiner can normally be reached on Monday - Friday, 8 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amelia Au can be reached on 703-308-6604. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

rjh
November 25, 2002

SAMIR AHMED
PRIMARY EXAMINER